

RAFAEL GARCIA

ragarcia@ufl.edu

Permanent Address:

1503 NW 17 ST
Gainesville, FL 32605
352-219-1696 (Cell)

OBJECTIVE: Seeking a full-time position in computer engineering, with special interest in High Performance Embedded Computing

EDUCATION

Master of Science, Electrical & Computer Engineering

University of Florida, Gainesville, Florida

Concentrations: Computer Architecture, Digital Signal Processing

May 2009

GPA: 3.8/4.0

Bachelor of Science, Electrical & Computer Engineering

University of Florida, Gainesville, Florida

May 2008

GPA: 3.8/4.0

WORK EXPERIENCE

Research Assistant, August 2007-Present

Center for High Performance Reconfigurable Computing (CHREC), Gainesville, Florida

- Developed tool for automated VHDL instrumentation using a complete Perl-based parser
- Created Kalman-filter based target tracking application on GiDEL ProcStar-II multi-FPGA platform in VHDL
- Implemented a standard framework for interfacing a heterogeneous FPGA-CPU cluster

PROJECTS

Integrated Product & Process Design (IPPD) project, August 2007-May 2008

Multidisciplinary project (5 student engineers) at UF funded by Honeywell ESEA

- Developed high-speed serial communication bit-error rate test-bed between Xilinx ML-205 FPGA boards
- Ported Linux to PowerPC architecture embedded in the Virtex4 FX-20 FPGA
- Contributed to design and creation of software/hardware fault injector to the 3.0 GB/s serial link
- Interfaced hardware components to a web-based GUI running locally on FPGA, allowing direct control of the bit error rate tester

Intelligent Machine Design Laboratory, Summer 2007

Designed and constructed a fully autonomous robot that scanned for coins on the ground, picked them up, counted and sorted them into individual coin tubes.

- Single-semester project with an 'A' final course grade
- Controlled and interfaced three sensor types (bump switches, IR proximity sensors, and color camera), two independent motor drivers, LCD screen, speaker, LEDs, and 12 button keypad to a single Atmel microcontroller
- Developed robust algorithm for detecting coin denomination based on size & color combination from on-board camera images
- Un-tethered, fully autonomous design running on 5 AA batteries
- Utilized innovative pulley/servo mechanism with plastic scoops for reliably picking up coins

COURSE WORK

Digital Filtering (grade earned: A), Fall 2008

- Obtained a foundation for digital filter design, analysis, implementation, and application
- Studied sampling, quantization, FFT, FIR, windowing, LMS methods, IIR, cascade/parallel design, and multi-rate filters

Image Processing & Computer Vision (grade earned: A), Fall 2008

- Explored diverse topics in the field of image processing and computer vision such as
 - Efficient representation of image/video signals
 - Image acquisition, properties of human visual perception, object recognition
 - Image de-blurring, edge detections, geometric transformations, video standards

Advanced Data Structures (grade earned: A), Summer 2008

- Learned about a variety of advanced data structures such as Huffman trees, priority queues, leftist trees, binomial heaps, AVL trees, red-black trees, B-/B+/B* trees, bloom filters, and others

Reconfigurable Computing (grade earned: A), Fall 2007

- Created a fully pipelined, systolic architecture for a low pass image filtering algorithm employing a 3x3 sliding window across a circular FIFO

Digital Computer Architecture Course (grade earned: A), Spring 2007

- Designed a 32-bit MIPS based pipelined processor using Altera's Quartus II software
- Implementation contained hazard detection and branch prediction

SKILLS

Computer Languages: C, C++, Java, Perl, MPI, UPC, VHDL

Software: Xilinx ISE, Altera Quartus II, Cadence Virtuoso Platform, Matlab, Blender3D

Language: Fluent in Spanish

AWARDS

Member, Golden Key International Honor Society, 2006-Present

Named to the College of Engineering Dean's List, 2006

University of Florida President's Honor Roll, 2004

PUBLICATIONS

- R. Garcia, A. Gordon-Ross, and A. George, "Exploiting Partially Reconfigurable FPGAs for Situation-Based Reconfiguration in Wireless Sensor Networks," *Proc. of 17th IEEE Symposium on Field-Programmable Custom Computing Machines (FCCM)*, Palo Alto, CA, Apr. 5-7, 2009 (short paper)
- J. Curreri, S. Koehler, A. George, B. Holland, and R. Garcia, "Performance Analysis Framework for High-Level Language Applications in Reconfigurable Computing," *ACM Transactions on Reconfigurable Technology and Systems (TRETs)*